FIG.1

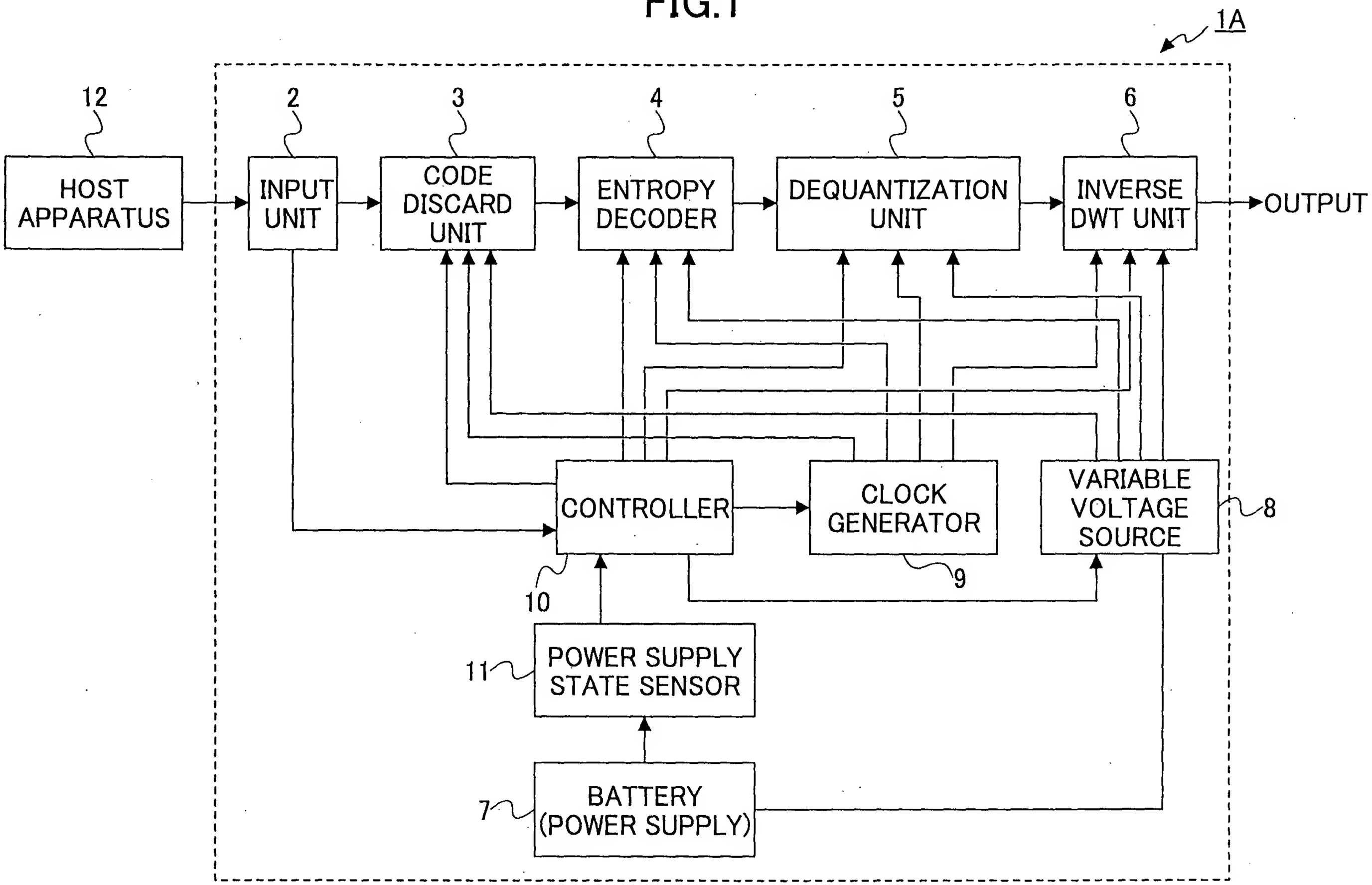

1A
12
HOST APPARATUS
2
INPUT UNIT
3
CODE DISCARD UNIT
4
ENTROPY DECODER
5
DEQUANTIZATION UNIT
6
INVERSE DWT UNIT
OUTPUT
CONTROLLER
CLOCK GENERATOR
VARIABLE VOLTAGE SOURCE
8
9
10
11
POWER SUPPLY STATE SENSOR
7
BATTERY (POWER SUPPLY)

FIG.2

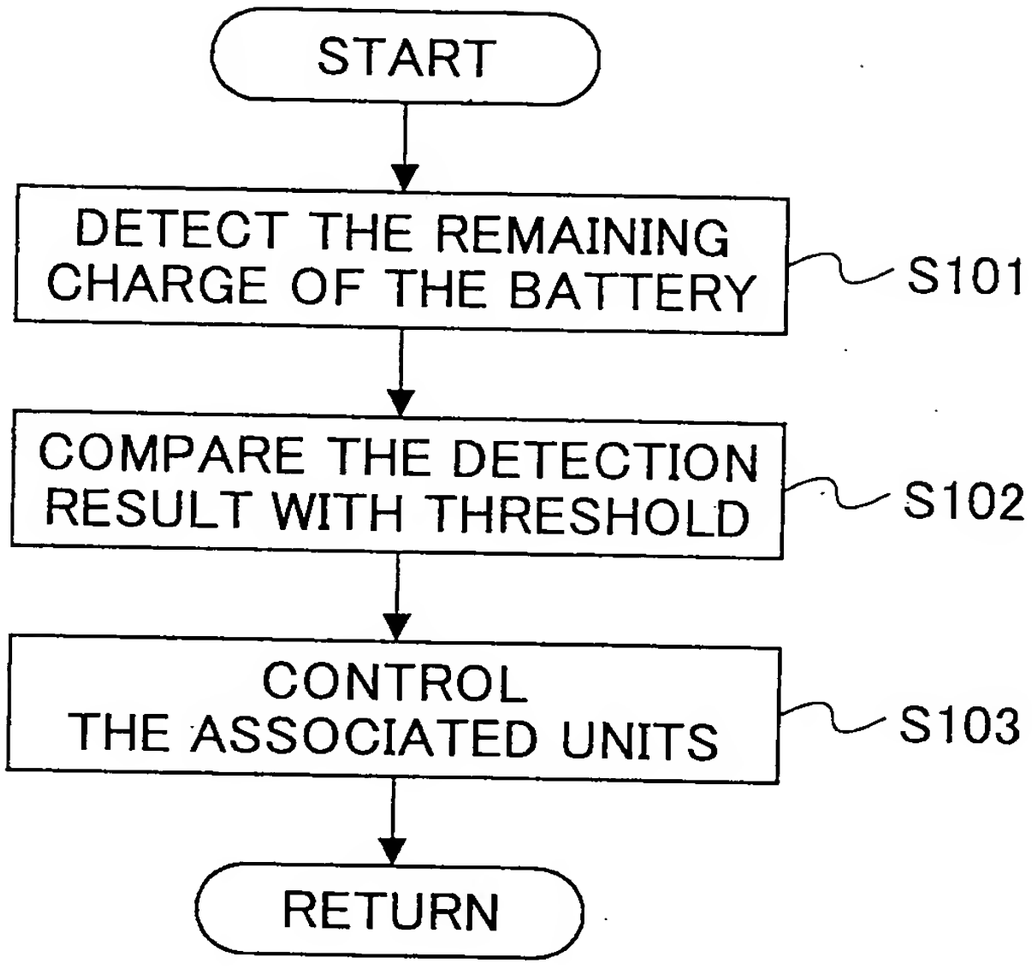

START
DETECT THE REMAINING CHARGE OF THE BATTERY
S101
COMPARE THE DETECTION RESULT WITH THRESHOLD
S102
CONTROL THE ASSOCIATED UNITS
S103
RETURN

FIG.3

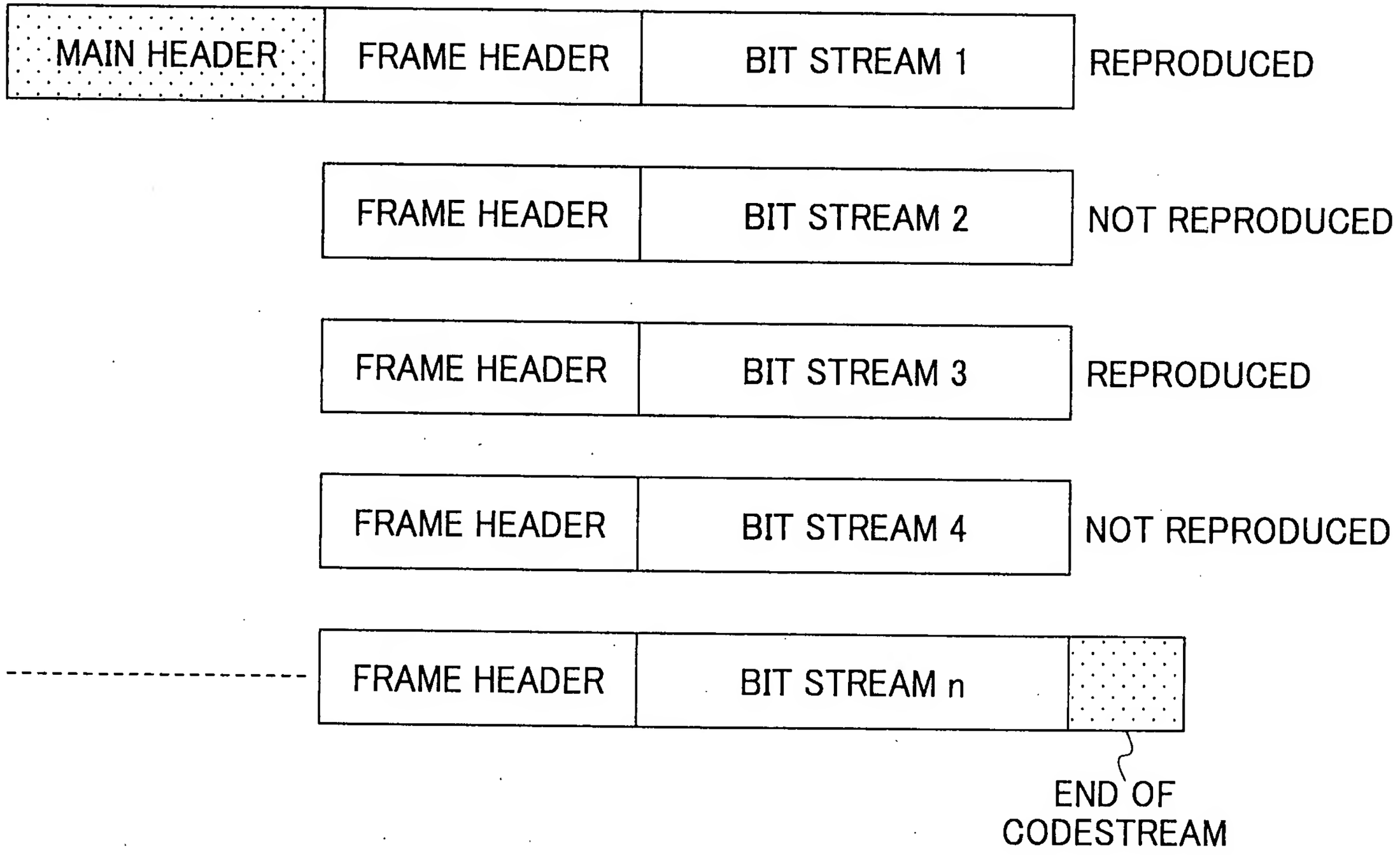

MAIN HEADER
FRAME HEADER
BIT STREAM 1
REPRODUCED
FRAME HEADER
BIT STREAM 2
NOT REPRODUCED
FRAME HEADER
BIT STREAM 3
REPRODUCED
FRAME HEADER
BIT STREAM 4
NOT REPRODUCED
FRAME HEADER
BIT STREAM n
END OF
CODESTREAM

FIG.4

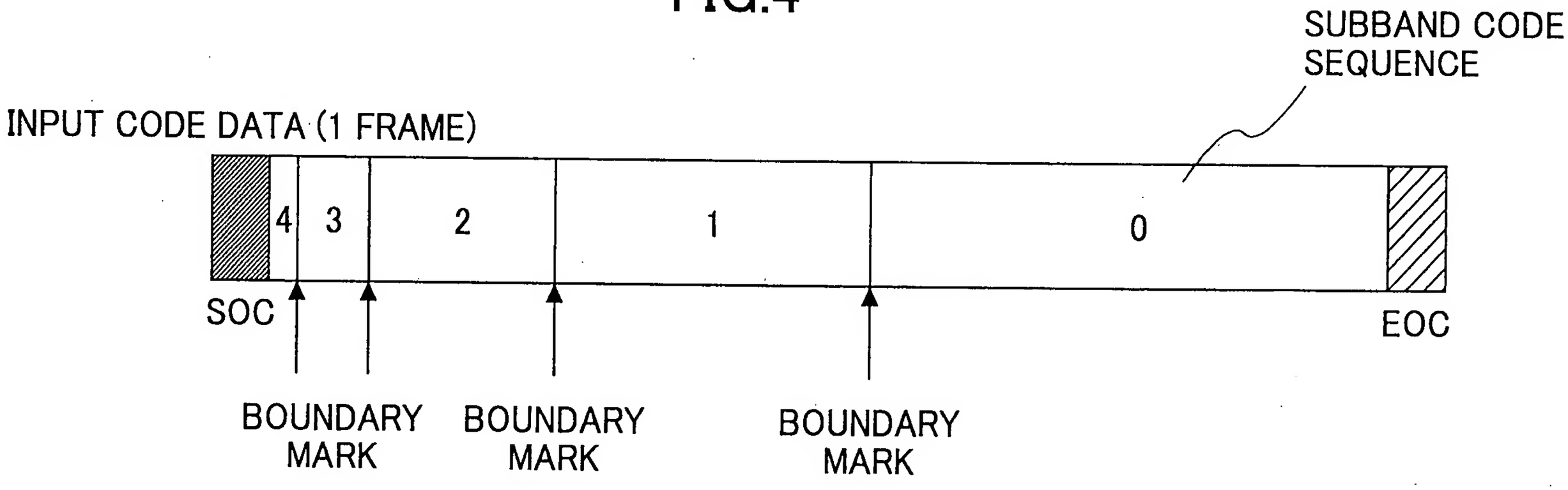

SUBBAND CODE SEQUENCE
INPUT CODE DATA (1 FRAME)
4
3
2
1
0
SOC
EOC
BOUNDARY MARK
BOUNDARY MARK
BOUNDARY MARK

FIG.5

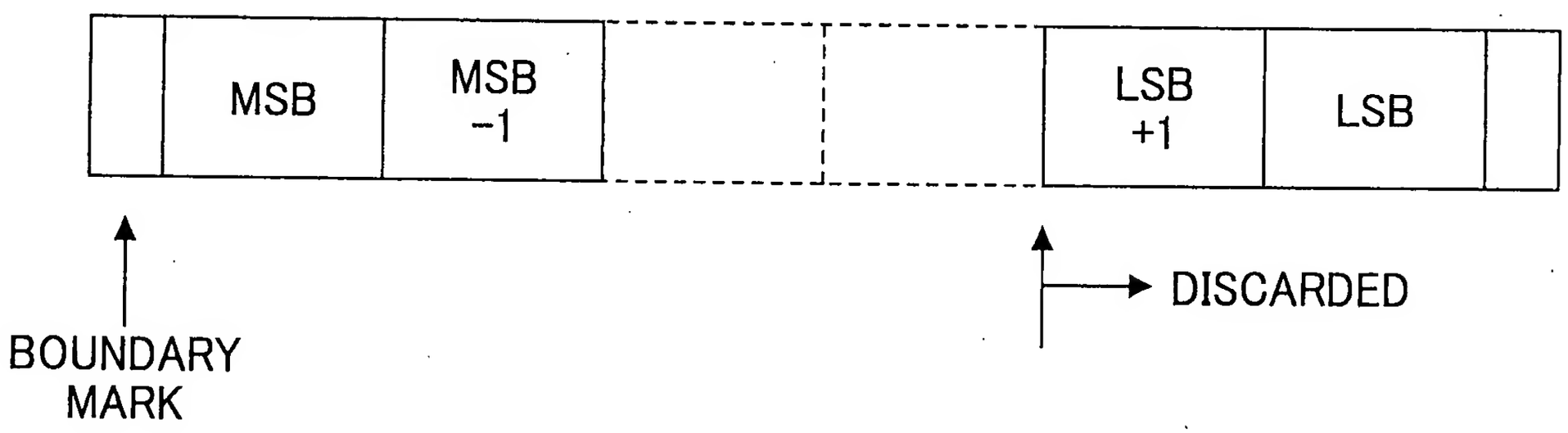

MSB
MSB -1
LSB +1
LSB
BOUNDARY MARK
DISCARDED

FIG.6A

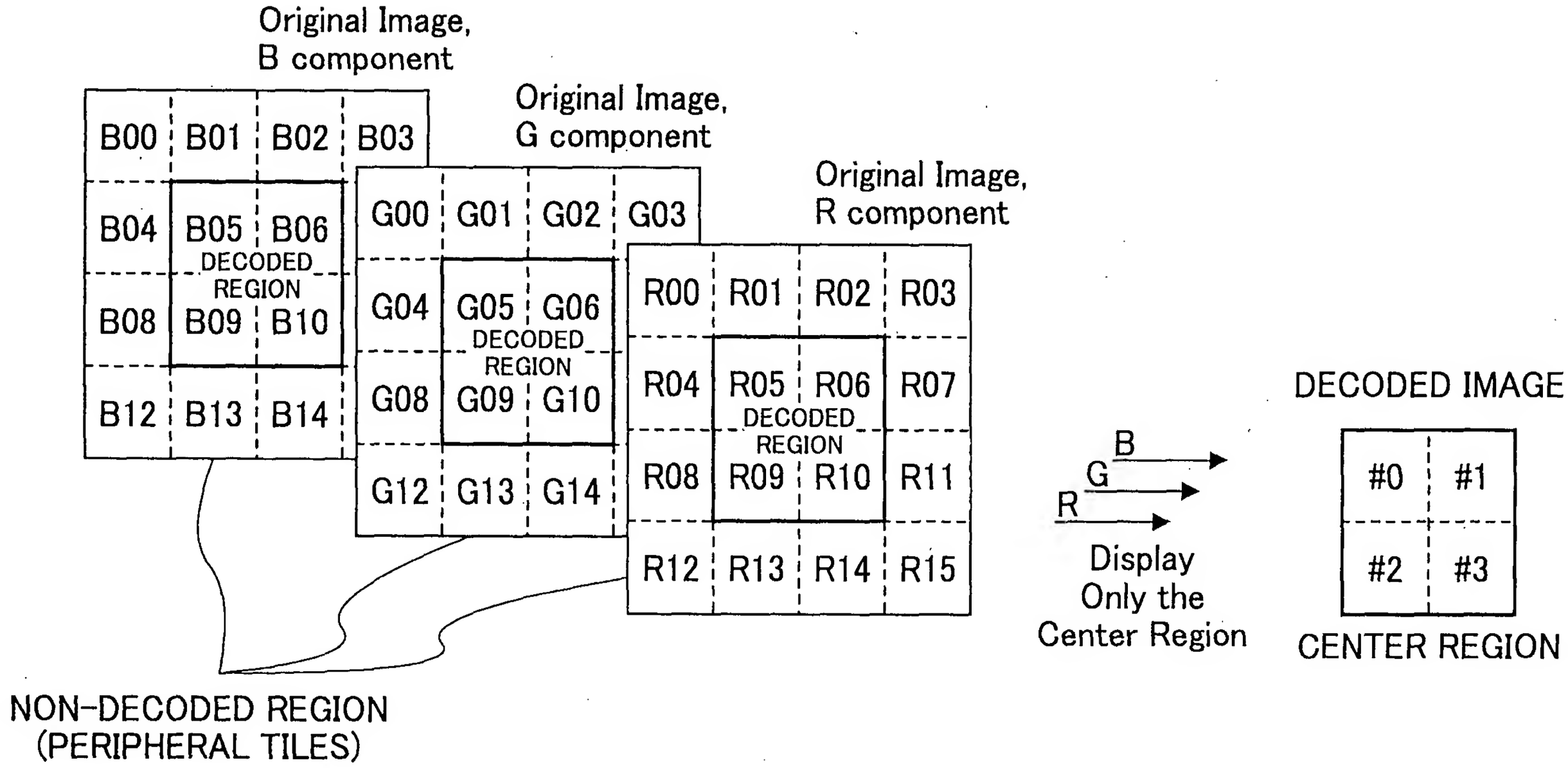

Original Image,
B component
B00
B01
B02
B03
B04
B05
B06
DECODED
REGION
B08
B09
B10
B12
B13
B14
Original Image,
G component
G00
G01
G02
G03
G04
G05
G06
DECODED
REGION
G08
G09
G10
G12
G13
G14
Original Image,
R component
R00
R01
R02
R03
R04
R05
R06
R07
DECODED
REGION
R08
R09
R10
R11
R12
R13
R14
R15
NON-DECODED REGION
(PERIPHERAL TILES)
B
G
R
Display
Only the
Center Region
DECODED IMAGE
#0
#1
#2
#3
CENTER REGION

FIG.6B

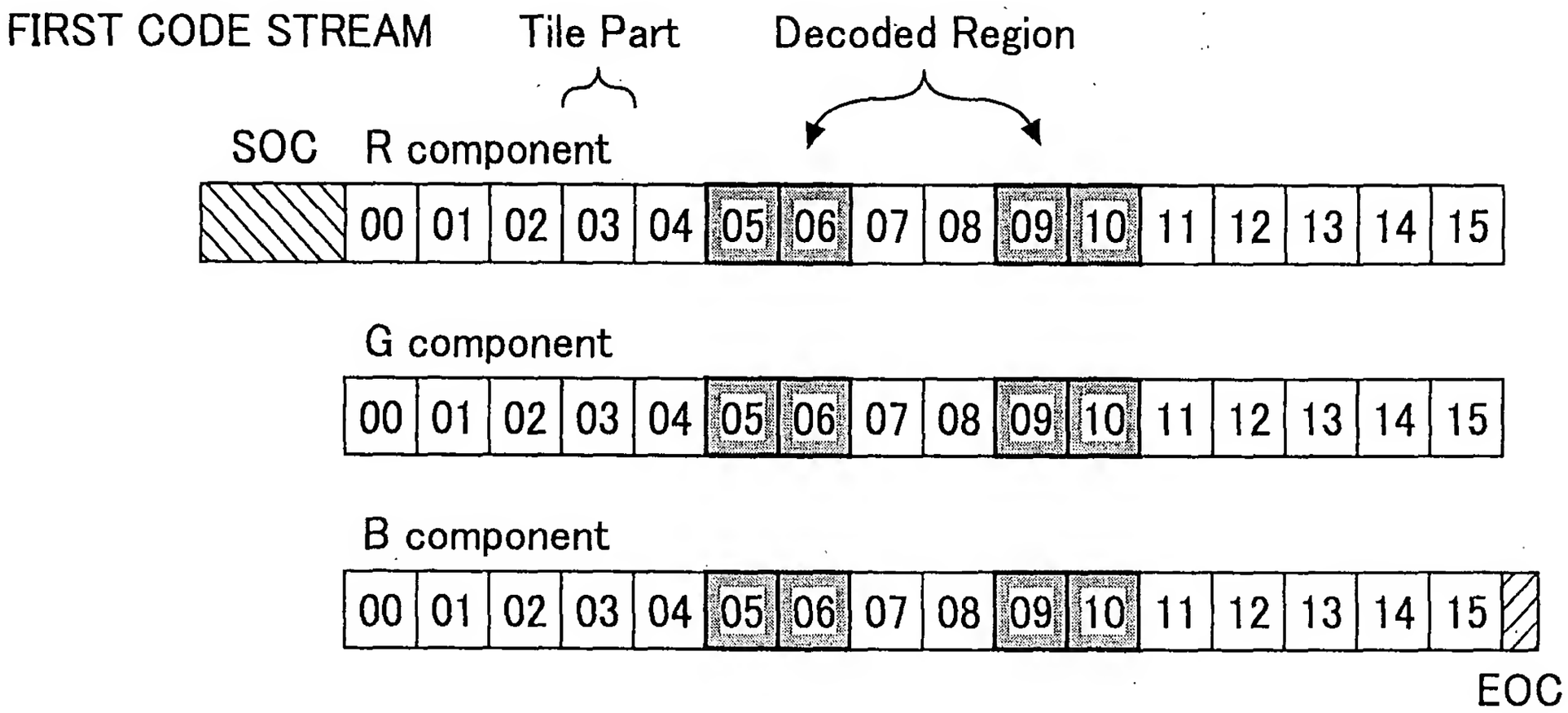

FIRST CODE STREAM
Tile Part
Decoded Region
SOC
R component
00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15
G component
00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15
B component
00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15
EOC

FIG.7

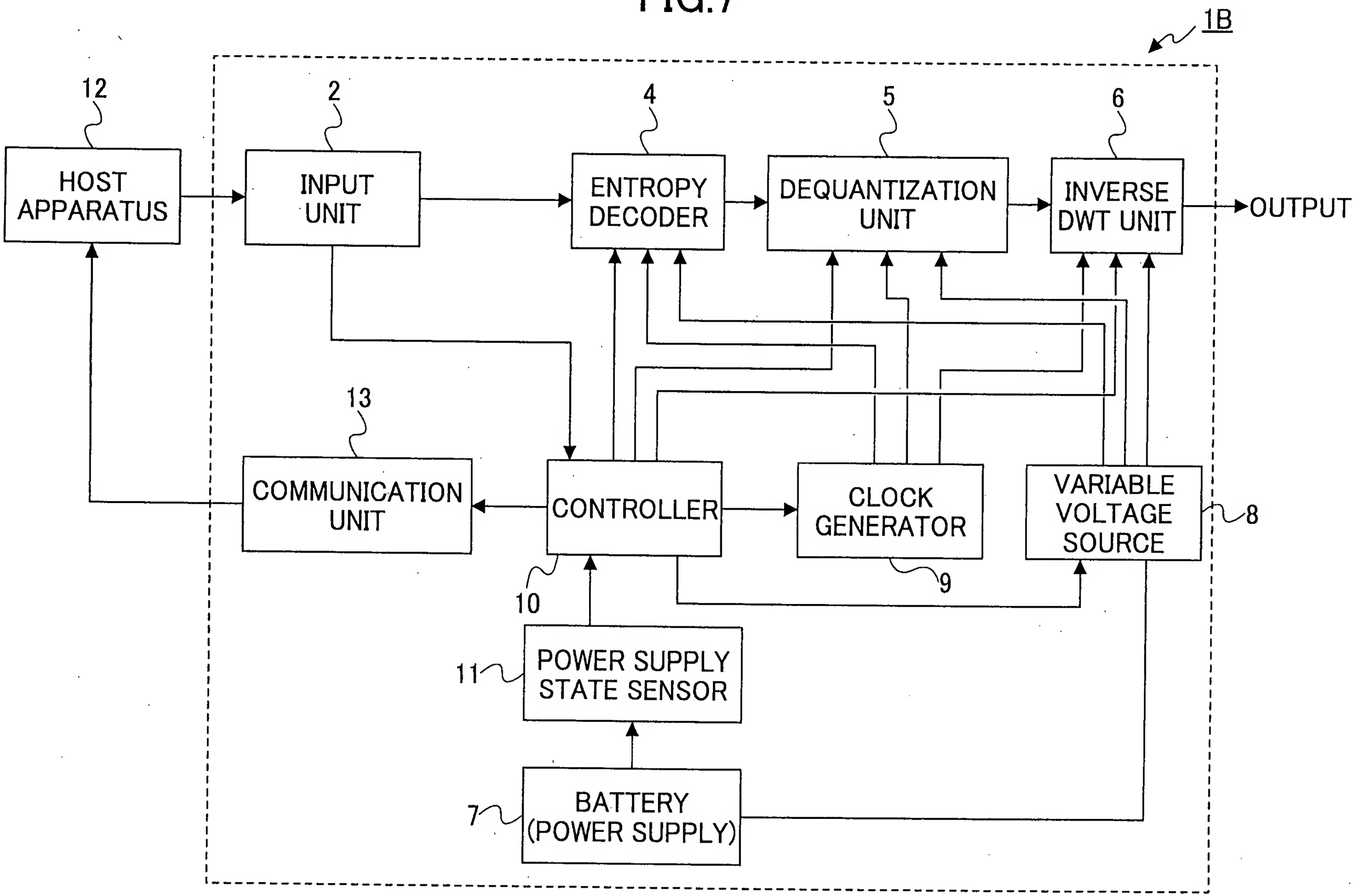

1B
12
2
4
5
6
HOST APPARATUS
INPUT UNIT
ENTROPY DECODER
DEQUANTIZATION UNIT
INVERSE DWT UNIT
OUTPUT
13
COMMUNICATION UNIT
CONTROLLER
CLOCK GENERATOR
VARIABLE VOLTAGE SOURCE
8
10
9
11
POWER SUPPLY STATE SENSOR
7
BATTERY (POWER SUPPLY)

FIG.8

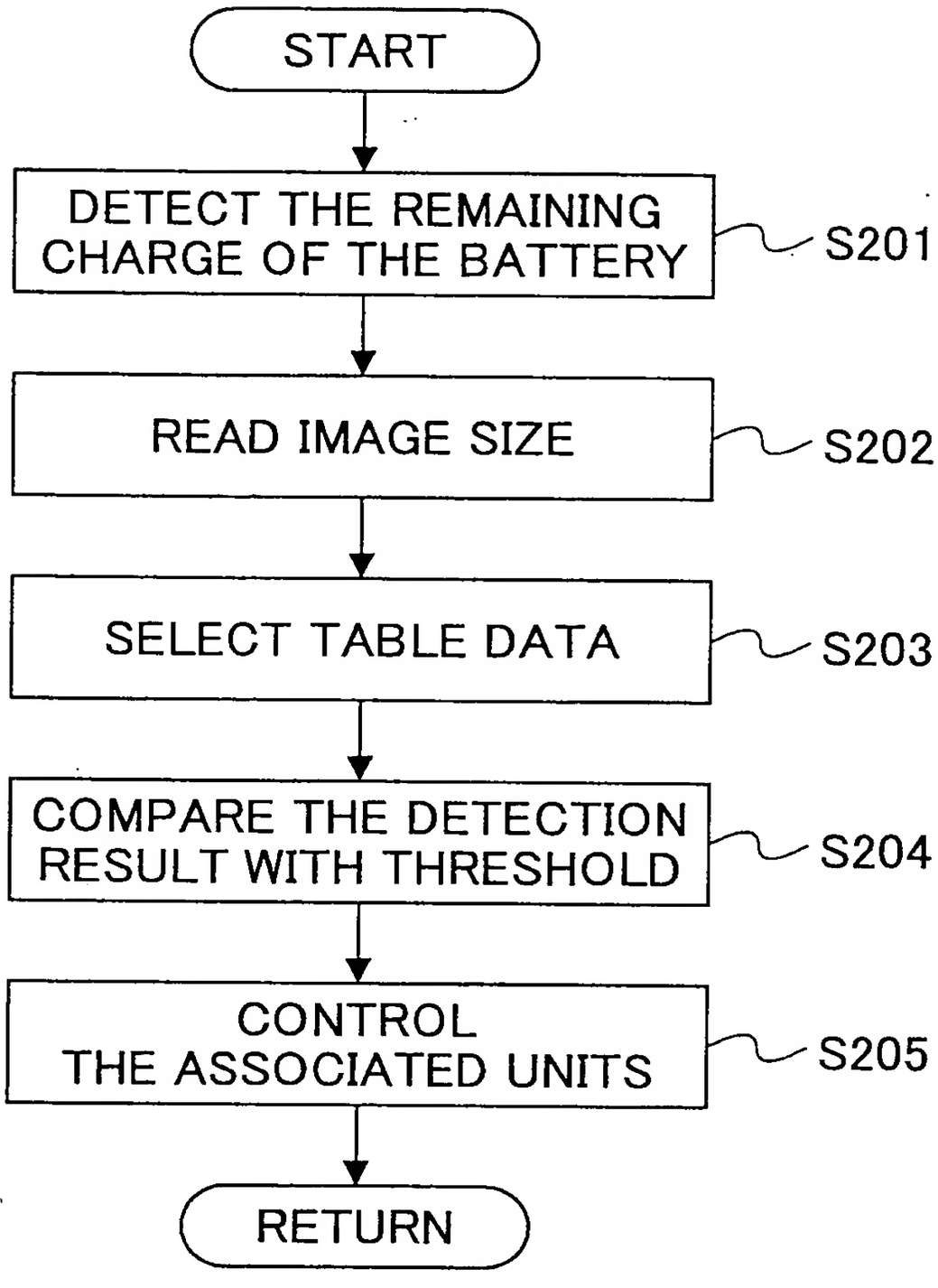

START
DETECT THE REMAINING CHARGE OF THE BATTERY
S201
READ IMAGE SIZE
S202
SELECT TABLE DATA
S203
COMPARE THE DETECTION RESULT WITH THRESHOLD
S204
CONTROL THE ASSOCIATED UNITS
S205
RETURN

FIG.9

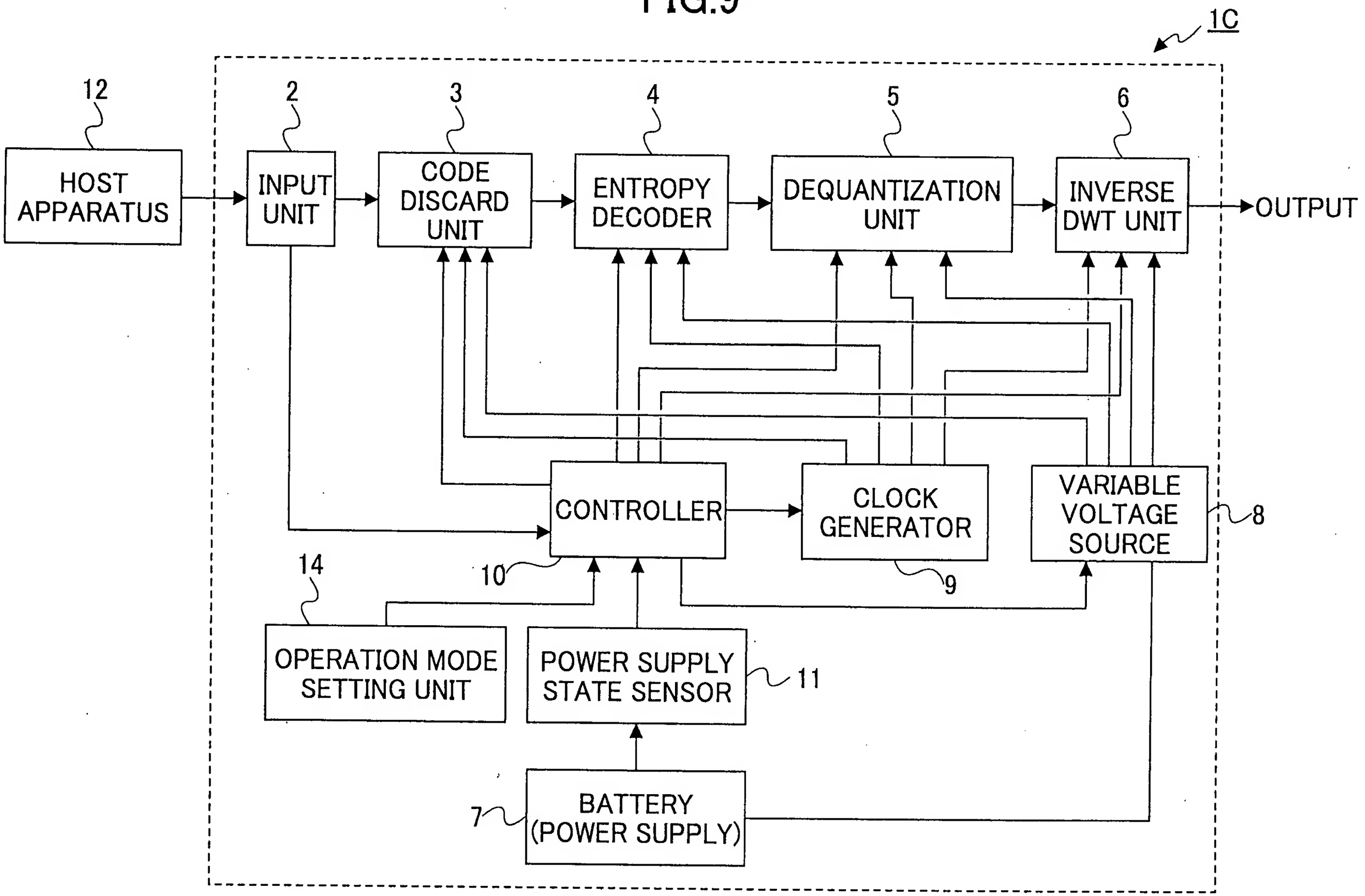

1C
12
HOST APPARATUS
2
INPUT UNIT
3
CODE DISCARD UNIT
4
ENTROPY DECODER
5
DEQUANTIZATION UNIT
6
INVERSE DWT UNIT
OUTPUT
CONTROLLER
10
CLOCK GENERATOR
9
VARIABLE VOLTAGE SOURCE
8
14
OPERATION MODE SETTING UNIT
POWER SUPPLY STATE SENSOR
11
7
BATTERY (POWER SUPPLY)

FIG.10

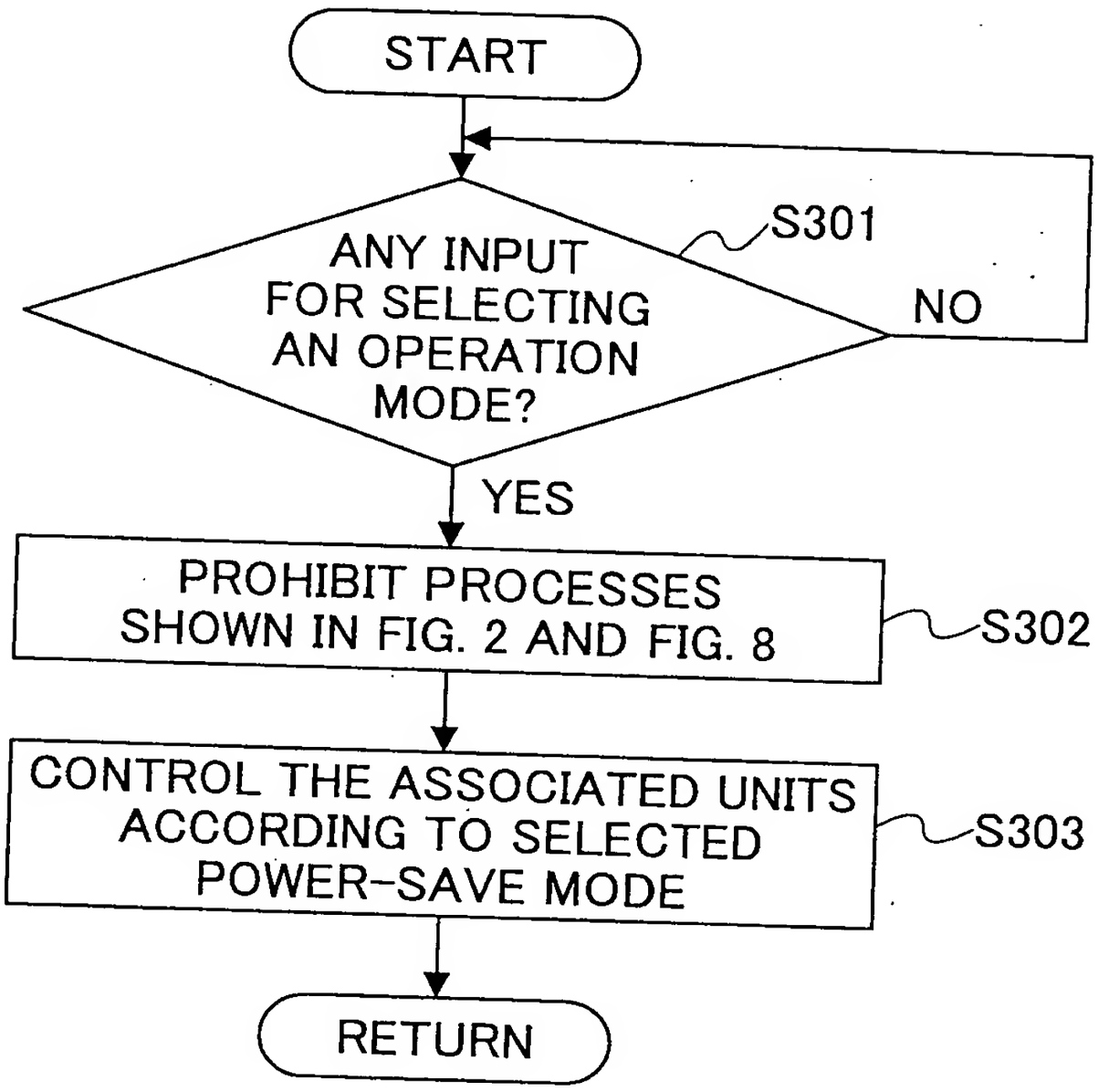

START
ANY INPUT FOR SELECTING AN OPERATION MODE?
S301
NO
YES
PROHIBIT PROCESSES SHOWN IN FIG. 2 AND FIG. 8
S302
CONTROL THE ASSOCIATED UNITS ACCORDING TO SELECTED POWER-SAVE MODE
S303
RETURN

FIG.11

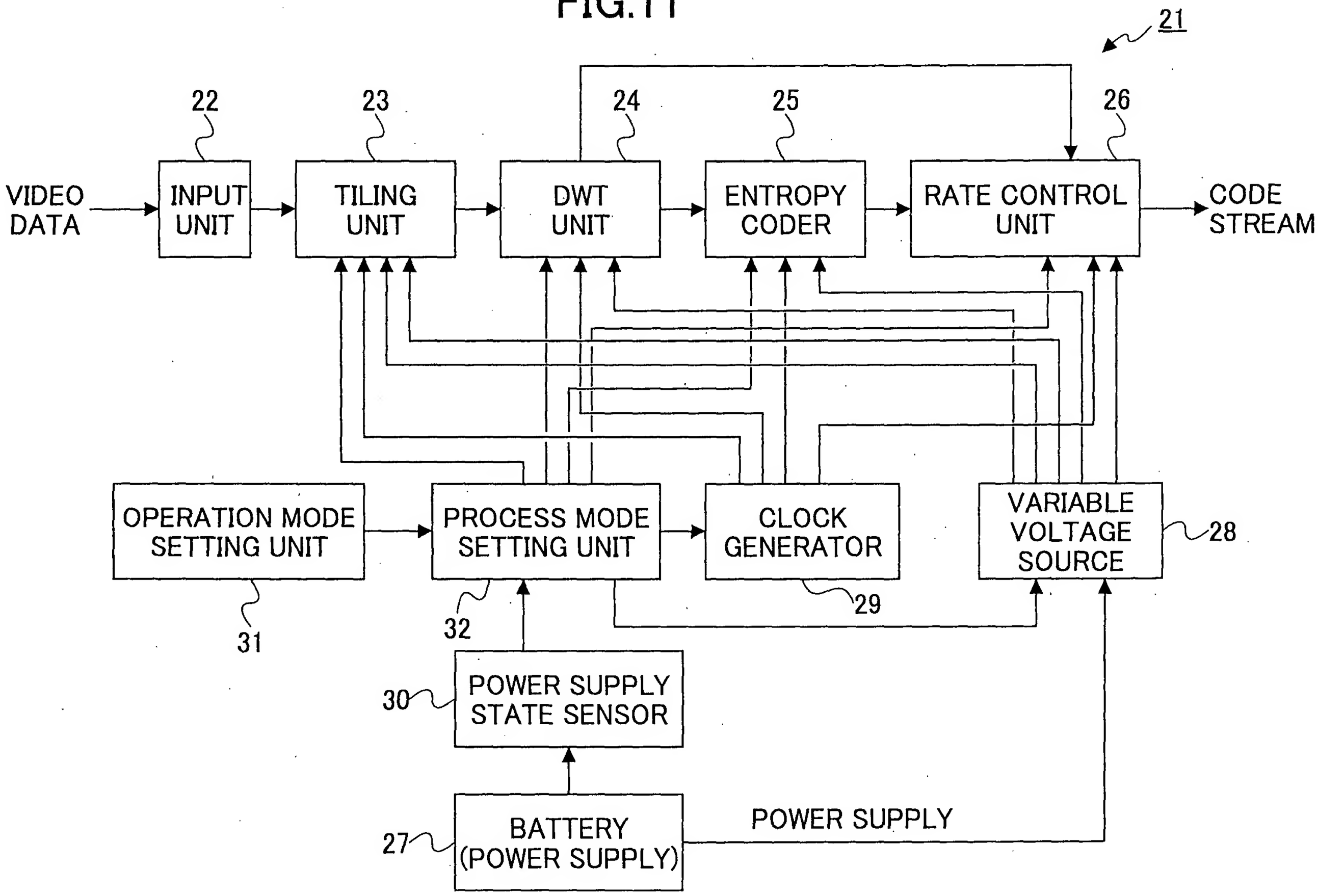

21
22
23
24
25
26
VIDEO DATA
INPUT UNIT
TILING UNIT
DWT UNIT
ENTROPY CODER
RATE CONTROL UNIT
CODE STREAM
OPERATION MODE SETTING UNIT
PROCESS MODE SETTING UNIT
CLOCK GENERATOR
VARIABLE VOLTAGE SOURCE
28
29
31
32
30
POWER SUPPLY STATE SENSOR
27
BATTERY (POWER SUPPLY)
POWER SUPPLY

FIG.12

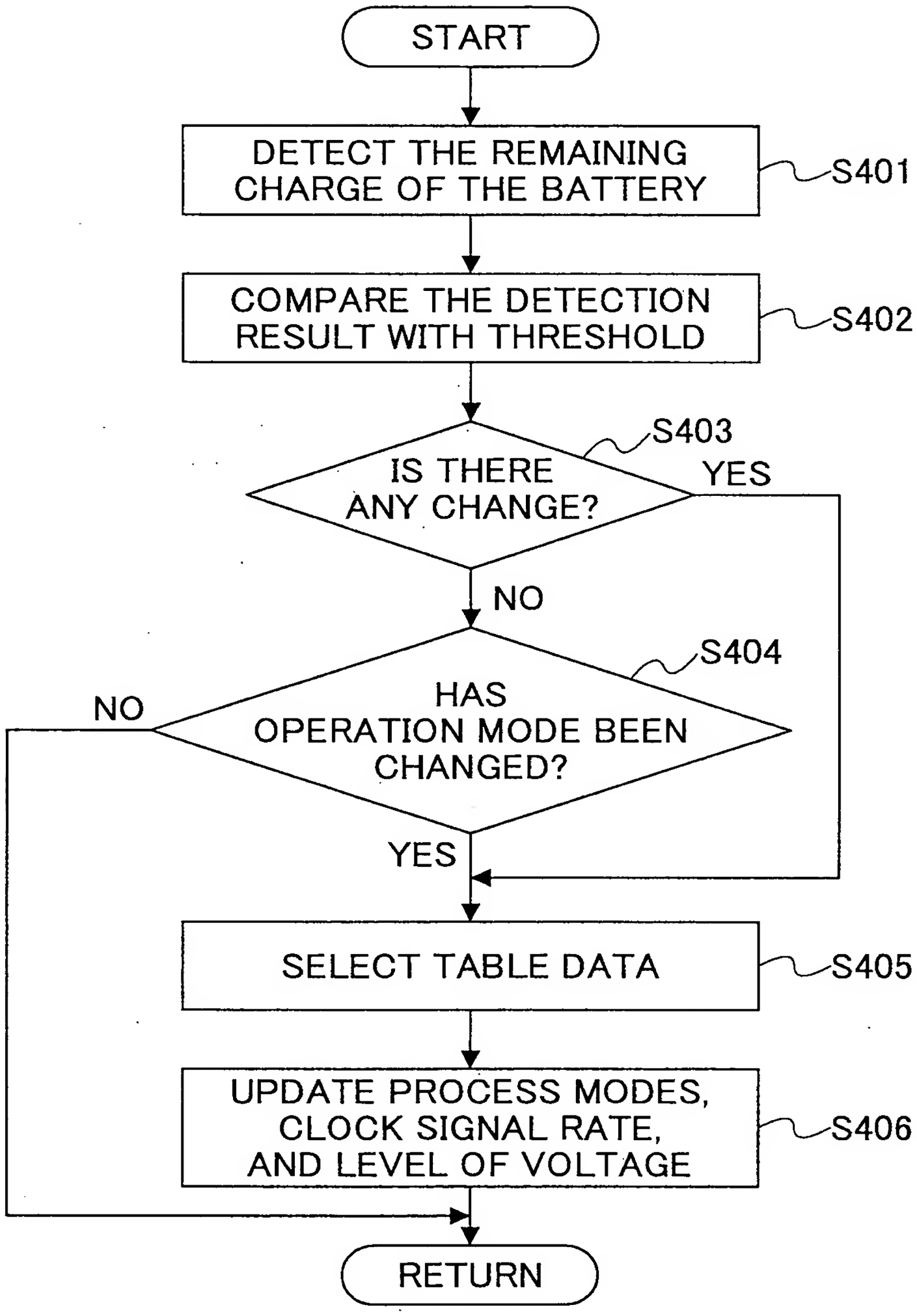

START
DETECT THE REMAINING CHARGE OF THE BATTERY
S401
COMPARE THE DETECTION RESULT WITH THRESHOLD
S402
S403
IS THERE ANY CHANGE?
YES
NO
S404
HAS OPERATION MODE BEEN CHANGED?
NO
YES
SELECT TABLE DATA
S405
UPDATE PROCESS MODES, CLOCK SIGNAL RATE, AND LEVEL OF VOLTAGE
S406
RETURN

FIG.13

POWER SUPPLY STATE (OPERATION MODE)	PROCESS MODE	CLOCK	OUTPUT VOLTAGE
AC (ORDINARY MODE)	OVERLAP 9*7 (5-LEVEL) LAGRANGIAN RATE CONTROL	1/1 CLOCK	3.3V
BATTERY CHARGE SUFFICIENT (POWER-SAVE MODE 1)	OVERLAP 9*7 (5-LEVEL) PLAIN RATE CONTROL	1/1 CLOCK	3.3V NO POWER SUPPLY FOR LAGRANGIAN RATE CONTROL
BATTERY CHARGE INSUFFICIENT (POWER-SAVE MODE 2)	NON-OVERLAP 5*3 (3-LEVEL) PLAIN RATE CONTROL	3/4 CLOCK	3.1V

34

FIG.14

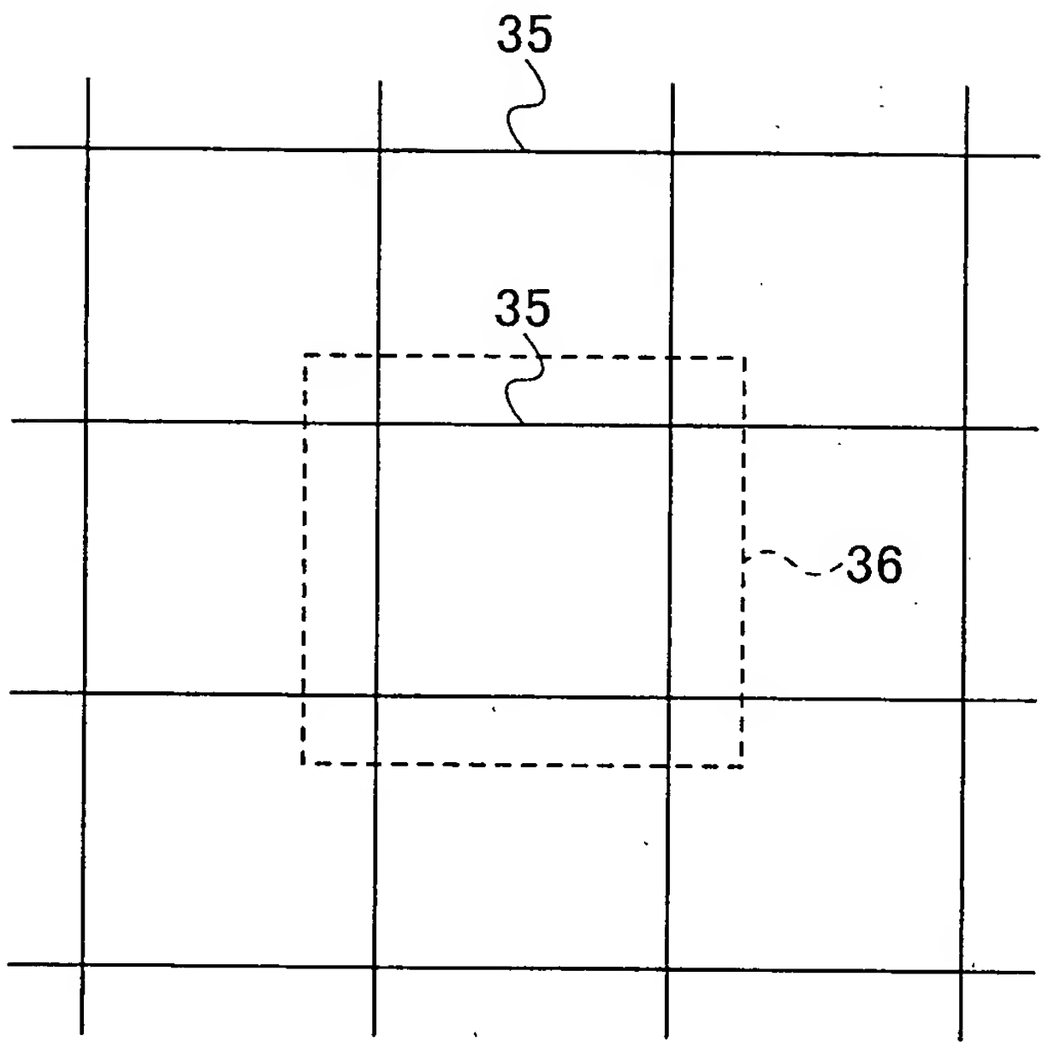
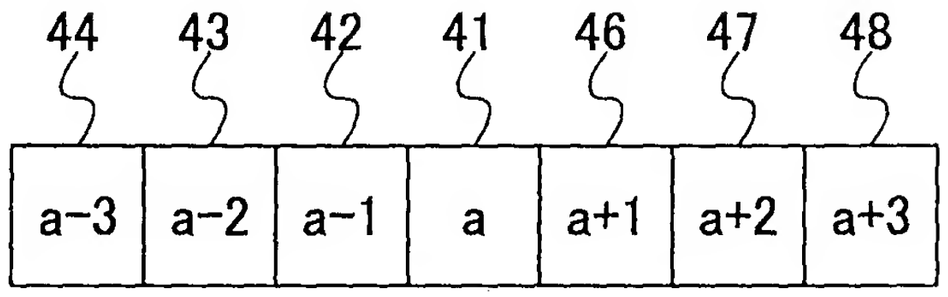


FIG.15A

9*7 FILTER:

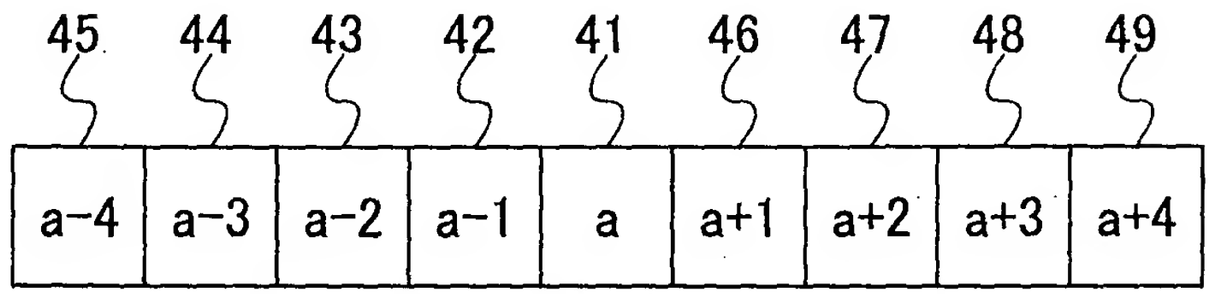
HIGH FREQUENCY COMPONENT



Coef. = A1*(a−3)+A2*(a−2)+A3*(a−1)+A4*a+A5*(a+1)+A6*(a+2)+A7*(a+3)

FIG.15B

LOW FREQUENCY COMPONENT

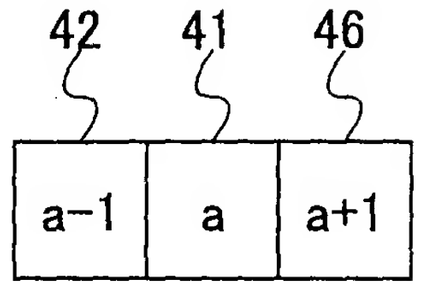


Coef. = B1*(a−4)+B2*(a−3)+B3*(a−2)+B4*(a−1)+B5*a+B6*(a+1)+B7*(a+2)+B8*(a+3)+B9*(a+4)

FIG.15C

5*3 FILTER:

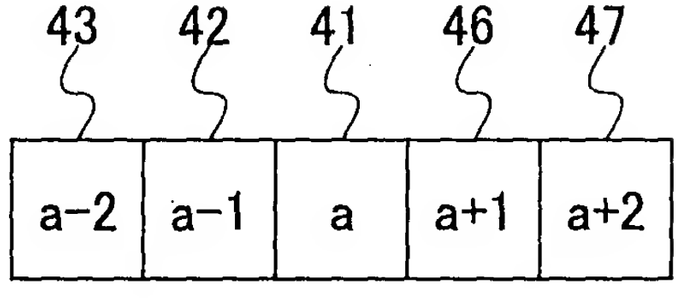
HIGH FREQUENCY COMPONENT



Coef. = D1*(a−1)+D2*a+D3*(a+1)

FIG.15D

LOW FREQUENCY COMPONENT



Coef. = E1*(a−2)+E2*(a−1)+E3*a+E4*(a+1)+E5*(a+2)

FIG.16A

3-Level Wavelet Decomposition

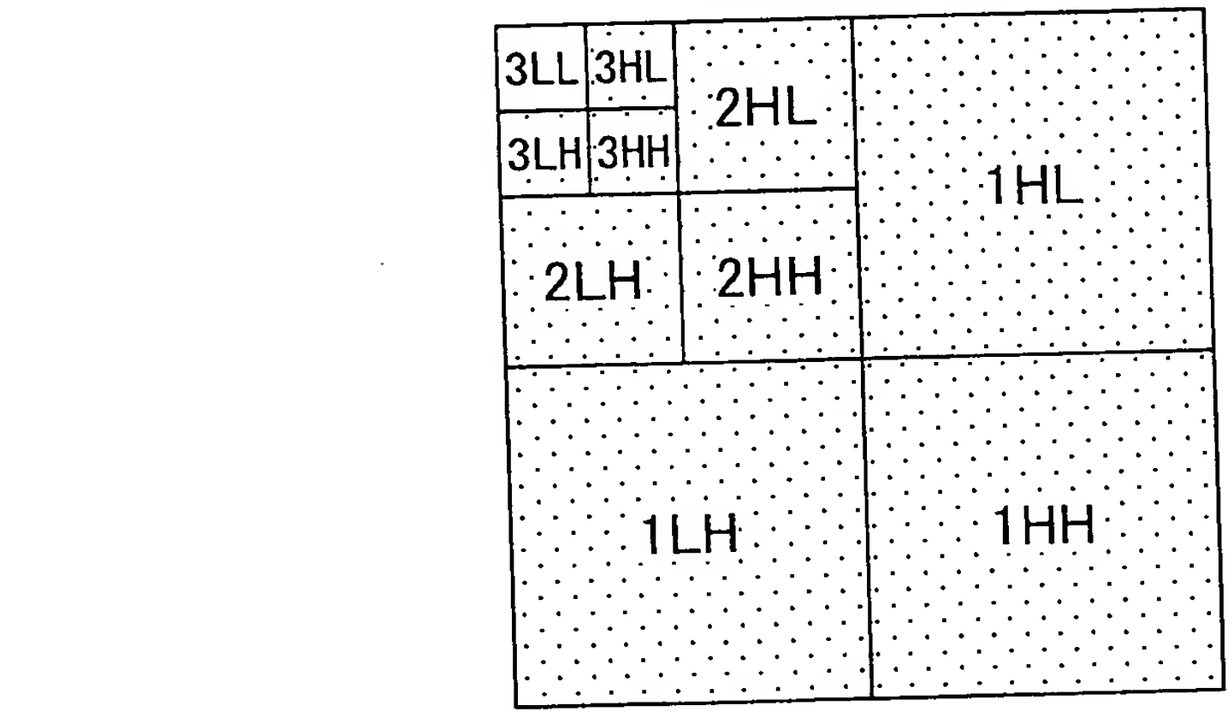


FIG.16B

5-Level Wavelet Decomposition

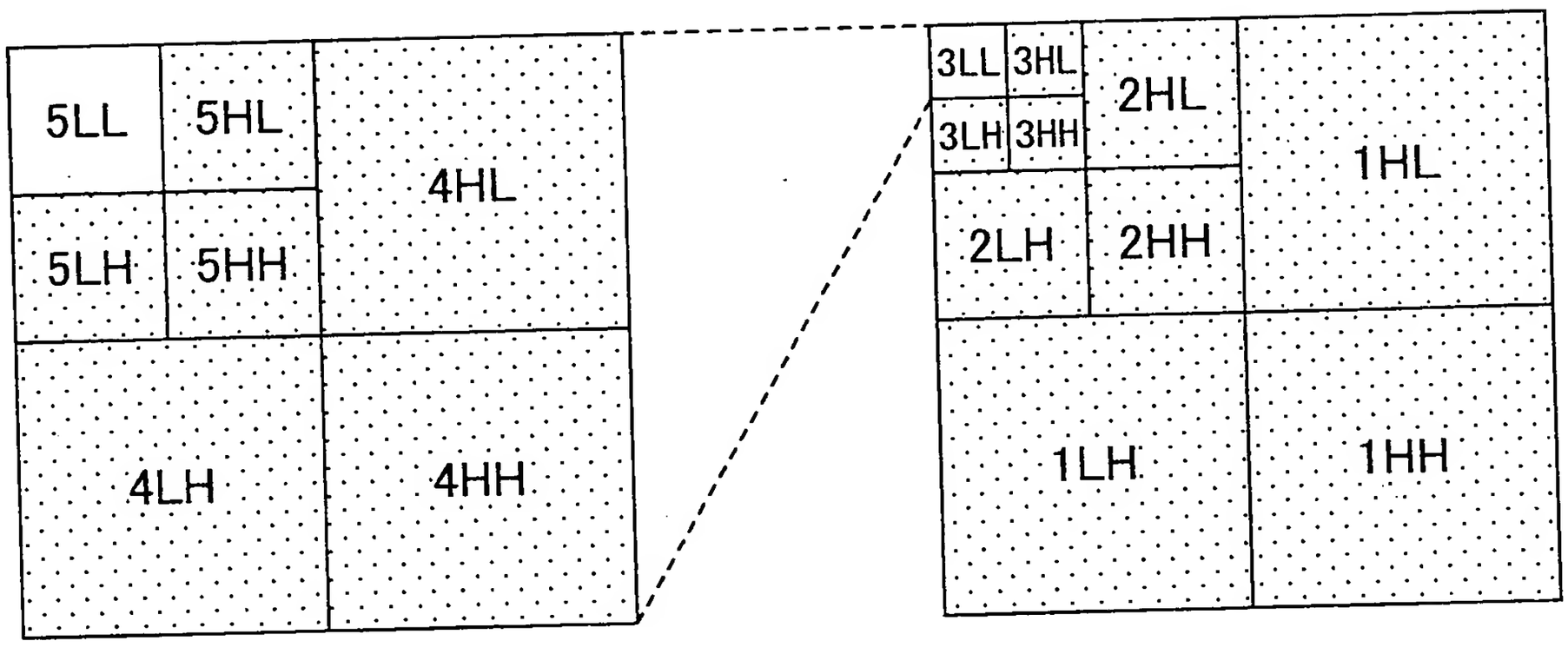


FIG.17

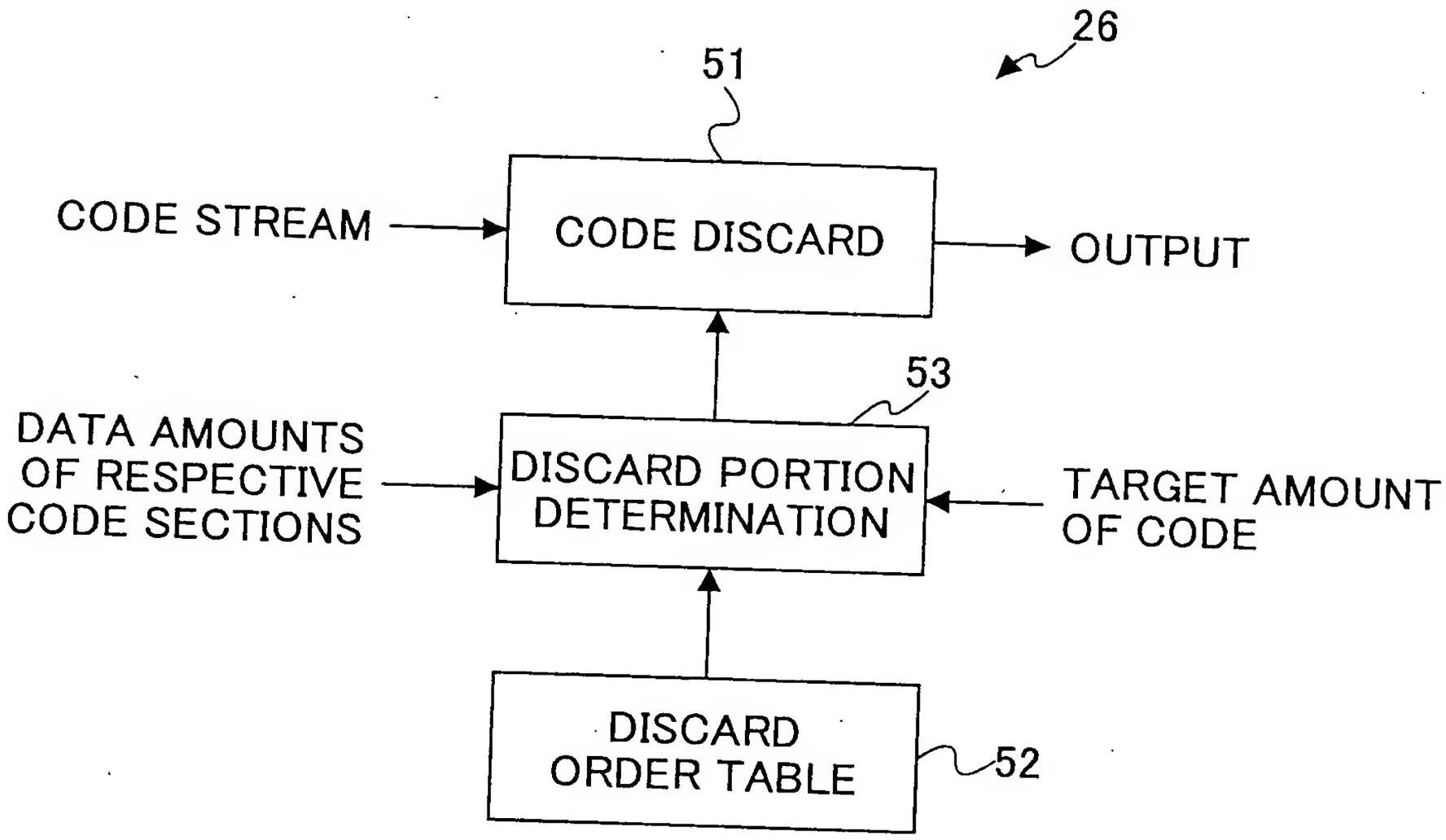

26
51
CODE STREAM
CODE DISCARD
OUTPUT
53
DATA AMOUNTS OF RESPECTIVE CODE SECTIONS
DISCARD PORTION DETERMINATION
TARGET AMOUNT OF CODE
DISCARD ORDER TABLE
52

FIG.18

DISCARD PATTERN #	2LL	2HL	2LH	2HH	1HL	1LH	1HH
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	0	2
3	0	0	0	0	0	0	3
4	0	0	0	0	0	1	3
5	0	0	0	0	1	1	3
6	0	0	0	0	1	1	4
7	0	0	0	0	1	2	4
8	0	0	0	0	2	2	4
...	...	...	...	...	...	...	...

DISCARD ORDER TABLE

FIG.19

2LL 2LL 2LL 2LL	2HL 2HL 2HL 2HL	1HL 1HL 1HL 1HL 1HL 1HL 1HL 1HL					
2LL 2LL 2LL 2LL	2HL 2HL 2HL 2HL	1HL 1HL 1HL 1HL 1HL 1HL 1HL 1HL					
2LL 2LL 2LL 2LL	2HL 2HL 2HL 2HL	1HL 1HL 1HL 1HL 1HL 1HL 1HL 1HL					
2LL 2LL 2LL 2LL	2HL 2HL 2HL 2HL	1HL 1HL 1HL 1HL 1HL 1HL 1HL 1HL					
2LH 2LH 2LH 2LH	2HH 2HH 2HH 2HH	1HL 1HL 1HL 1HL 1HL 1HL 1HL 1HL					
2LH 2LH 2LH 2LH	2HH 2HH 2HH 2HH	1HL 1HL 1HL 1HL 1HL 1HL 1HL 1HL					
2LH 2LH 2LH 2LH	2HH 2HH 2HH 2HH	1HL 1HL 1HL 1HL 1HL 1HL 1HL 1HL					
2LH 2LH 2LH 2LH	2HH 2HH 2HH 2HH	1HL 1HL 1HL 1HL 1HL 1HL 1HL 1HL					
1LH 1LH 1LH 1LH	1LH 1LH 1LH 1LH	1HH 1HH 1HH 1HH 1HH 1HH 1HH 1HH					
1LH 1LH 1LH 1LH	1LH 1LH 1LH 1LH	1HH 1HH 1HH 1HH 1HH 1HH 1HH 1HH					
1LH 1LH 1LH 1LH	1LH 1LH 1LH 1LH	1HH 1HH 1HH 1HH 1HH 1HH 1HH 1HH					
1LH 1LH 1LH 1LH	1LH 1LH 1LH 1LH	1HH 1HH 1HH 1HH 1HH 1HH 1HH 1HH					
1LH 1LH 1LH 1LH	1LH 1LH 1LH 1LH	1HH 1HH 1HH 1HH 1HH 1HH 1HH 1HH					
1LH 1LH 1LH 1LH	1LH 1LH 1LH 1LH	1HH 1HH 1HH 1HH 1HH 1HH 1HH 1HH					
1LH 1LH 1LH 1LH	1LH 1LH 1LH 1LH	1HH 1HH 1HH 1HH 1HH 1HH 1HH 1HH					
1LH 1LH 1LH 1LH	1LH 1LH 1LH 1LH	1HH 1HH 1HH 1HH 1HH 1HH 1HH 1HH					

COEFFICIENTS OF 2-LEVEL WAVELET TRANSFORM

FIG.20A

0	1	2	3
4	5	6	7
8	9	10	11
12	13	14	15

COEFFICIENTS OF 2LL SUBBAND

FIG.20B

0	0	0	0
0	0	0	0
1	1	1	1
1	1	1	1

0	0	0	0
1	1	1	1
0	0	0	0
1	1	1	1

0	0	1	1
0	0	1	1
0	0	1	1
0	0	1	1

0	1	0	1
0	1	0	1
0	1	0	1
0	1	0	1

HIGHEST BIT-PLANE

LOWEST BIT-PLANE

4 BIT-PLANES OF 2LL SUBBAND

FIG.21

2LL	CODE OF THE HIGHEST BIT-PLANE
	...
	CODE OF THE LOWEST BIT-PLANE
2HL	CODE OF THE HIGHEST BIT-PLANE
	...
	CODE OF THE LOWEST BIT-PLANE
2LH	CODE OF THE HIGHEST BIT-PLANE
	...
	CODE OF THE LOWEST BIT-PLANE
2HH	CODE OF THE HIGHEST BIT-PLANE
	...
	CODE OF THE LOWEST BIT-PLANE
1HL	CODE OF THE HIGHEST BIT-PLANE
	...
	CODE OF THE LOWEST BIT-PLANE
1LH	CODE OF THE HIGHEST BIT-PLANE
	...
	CODE OF THE LOWEST BIT-PLANE
1HH	CODE OF THE HIGHEST BIT-PLANE
	...
	CODE OF THE LOWEST BIT-PLANE